Notice of Allowability	Application No.	Applicant(s)	
	10/047,344	WU ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/16/05*.

2. ☒ The allowed claim(s) is/are *1-13*.

3. ☒ The drawings filed on *15 January 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

Examiner's statement for reason for allowance

The following is an examiner's statement for allowance:

1. Claims **1-13** have been allowed.

As per claim 1:

The prior art (Saw et al. (U.S. PN: 5,345,450)) of record in figure 7 teach a flow chart of a method utilized for reducing the simulation time and data storage requirements for a computer simulation of a logic device, where the simulation involves a series of redundant input and expected output vectors (see col. 5, lines 43-48). Saw et al. in step 1040, teach a reduced set of input vectors is generated for simulation from the sequence of input vectors selected in step (1010), by eliminating all but the first of the redundant input vectors in the series of redundant input vectors having the same expected output vectors (see col. 6, lines 38-52), in step (1060), the reduced set of input vectors are then provided to a computer simulation (e.g., 100 in FIG. 8A) of the logic device 10 along with the associated control bits (e.g., CB1 and CB2) of each input vector, as schematically illustrated in FIG. 8A, in order to generate the corresponding expected output vectors for each of those input vectors. However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method for selecting an optimal test sequence from a sequence of N tests comprising the steps for each test of the a sequence of N tests, compiling test results for L defective dice, wherein said N tests comprise one or more redundant tests and one or more inefficient tests; representing each test of they sequence of N tests as a correlation vector of length L, such that the sequence of N tests is represented as N correlation vectors, wherein element i of correlation vector for test i is zero if

device i passed test i finding a first correlation vector of the N correlation vectors that has the most non-zero components and a vector W to be the complement of the first: correlation vector; selecting a first test in the optimal test sequence to be the test represented by the first correlation vector; for each correlation vector of the remaining N-1 correlation vectors, calculating a product: of the complement of each correlation vector and the vector W; calculating a length of a projection of each calculated product vector onto a unit vector; finding a next correlation vector that is the correlation vector of the N-1 correlation vectors that: has a smallest value of the projection length; selecting a next test in the optimal test sequence to be the test represented by the next correlation vector; updating the vector W to be a product of vector W and a compliment of the determined correlation vector in the previous step; and repeating the previous five few elements, until the length of the projection of vector W onto the unit vector is zero. Consequently, claim 1 is allowed over the prior art.

Claims 2-10, which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 11:

The prior art (Saw et al. (U.S. PN: 5,345,450)) of record in figure 7 teach a flow chart of a method utilized for reducing the simulation time and data storage requirements for a computer simulation of a logic device, where the simulation involves a series of redundant input and expected output vectors (see col. 5, lines 43-48). Saw et al. in step 1040, teach a reduced set of input vectors is generated for simulation from the sequence of input vectors selected in step (1010), by eliminating all but the first of the redundant input vectors in the series of redundant input vectors having the same expected output vectors (see col. 6, lines 38-52), in step (1060),

the reduced set of input vectors are then provided to a computer simulation (e.g., 100 in FIG. 8A) of the logic device 10 along with the associated control bits (e.g., CB1 and CB2) of each input vector, as schematically illustrated in FIG. 8A, in order to generate the corresponding expected output vectors for each of those input vectors. However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method for the reordering a sequence of N tests for detecting faults in digital integrated circuits (IC's) as an optimal sequence of tests when the execution time of each test is the same, comprising the steps of for each test of the a sequence of N tests, compiling test results for L defective dice; representing each test of the sequence of N tests as a correlation vector using a binary-valued L-dimensional vector, wherein bit i of correlation vector for test i is zero if device i passed test i; finding a first correlation vector of the N correlation vectors that has the most non-zero components and initializing a vector W to be the complement of this first: correlation vector; storing the test represented by the first correlation vector as a first test in the optimal sequence of tests: defining a multiplication of two correlation vectors to be a vector with components calculated from the logical AND operation of the corresponding components of the two correlation vectors; for each correlation vector of the remaining correlation vectors, calculating a product vector of the complement of each correlation vector and vector W using the multiplication definition in the previous element; calculating a projection length of each product vector onto the unit vector; finding a next correlation vector that is the correlation vector that has the smallest value of the projection length; storing the test represented by the next this correlation vector as a test in as the optimized sequence of tests; updating vector W to be the product of vector W and a compliment of the correlation vector in the previous step; repeating the previous five elements, until the length of

the projection of vector W onto the unit vector is zero; and assigning the vector W to be the unit vector and repeating the previous six elements until there are no remaining vectors. Consequently, claim 11 is allowed over the prior art.

As per claim 12:

The prior art (Saw et al. (U.S. PN: 5,345,450)) of record in figure 7 teach a flow chart of a method utilized for reducing the simulation time and data storage requirements for a computer simulation of a logic device, where the simulation involves a series of redundant input and expected output vectors (see col. 5, lines 43-48). Saw et al. in step 1040, teach a reduced set of input vectors is generated for simulation from the sequence of input vectors selected in step (1010), by eliminating all but the first of the redundant input vectors in the series of redundant input vectors having the same expected output vectors (see col. 6, lines 38-52), in step (1060), the reduced set of input vectors are then provided to a computer simulation (e.g., 100 in FIG. 8A) of the logic device 10 along with the associated control bits (e.g., CB1 and CB2) of each input vector, as schematically illustrated in FIG. 8A, in order to generate the corresponding expected output vectors for each of those input vectors. However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method for the reordering a sequence of N tests as an optimal sequence of tests for detecting faults tests in digital integrated circuits (IC's) when the execution times of the each tests in the sequence of N tests are not all the same, comprising the steps for each test of the a sequence of N tests, compiling test results for L defective dice and storing the execution time of the sequence of N tests; representing each test of the sequence N tests as a correlation vector using a binary-valued L-dimensional vector, wherein bit i of correlation vector for test i is zero if device j passed test i; finding a first correlation

vector of the N correlation vectors that has the largest value of the number of non-zero components divided by the execution time of the corresponding test and then initialize vector W to be a complement of this vector; storing the test represented by the first correlation vector as a first test in the optimal sequence of tests; defining the multiplication of two correlation vectors to be a vector with components that are calculated from the logical AND operation of the corresponding components of the two correlation vectors; for each correlation vector of the remaining correlation vectors, calculating a length of a projection of the correlation vector onto vector W; calculating a quotient of the calculated projection length in the previous step and the execution time of the corresponding test; finding a next correlation vector that is the correlation vector that has the largest value of the quotient calculated in the previous step; storing the test represented by the next correlation vector as a test in the optimized sequence of tests; updating vector W to be the product of vector W and the compliment of the stored correlation vector in the previous step; and repeating the previous five elements, until the length of the projection of vector W onto the unit vector is zero. Consequently, claim 12 is allowed over the prior art.

As per claim 13:

The prior art (Saw et al. (U.S. PN: 5,345,450)) of record in figure 7 teach a flow chart of a method utilized for reducing the simulation time and data storage requirements for a computer simulation of a logic device, where the simulation involves a series of redundant input and expected output vectors (see col. 5, lines 43-48). Saw et al. in step 1040, teach a reduced set of input vectors is generated for simulation from the sequence of input vectors selected in step (1010), by eliminating all but the first of the redundant input vectors in the series of redundant input vectors having the same expected output vectors (see col. 6, lines 38-52), in step (1060),

the reduced set of input vectors are then provided to a computer simulation (e.g., 100 in FIG. 8A) of the logic device 10 along with the associated control bits (e.g., CB1 and CB2) of each input vector, as schematically illustrated in FIG. 8A, in order to generate the corresponding expected output vectors for each of those input vectors. However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a method for the reordering a sequence of N tests as an optimal sequence of tests for detecting faults tests in digital integrated circuits (IC's) when the execution times of the tests in the sequence of N tests are not all the same, comprising the steps for each test of a sequence of N tests, compiling test results for L defective dice and storing the execution time of the sequence of N tests; representing each test of the sequence of N tests as a correlation vector using a binary-valued L-dimensional vector, wherein bit j of correlation vector for test i is zero if device j passed test i; finding a first correlation vector of the N correlation vectors that has the largest value of the number of non-zero components divided by the execution time of the corresponding test and then initialize a vector W to be a complement of this vector; storing the test represented by tie first correlation vector as a first test in the optimal sequence of tests: defining a multiplication of two correlation vectors to be a vector with components that are calculated from the logical AND operation of the corresponding components of the two correlation vectors; for each correlation vector of the: remaining correlation vectors, calculating a length of a projection of the correlation vector onto vector W; calculating a quotient of the calculated projection length in the previous step and the execution time of the corresponding test; finding a next correlation vector that is a correlation vector that has the largest value of the quotient calculated in the previous step; storing the test represented by the next this correlation vector as a test in the optimized sequence of tests;

updating vector W to be the product of vector W and a compliment of the stored correlation vector in the previous step; repeating the previous five elements, until the length of the projection of vector W onto a unit vector is zero; and assigning vector W to be the unit vector and repeating the previous six elements until there are no remaining vectors. Consequently, claim 13 is allowed over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

2. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5. If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

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